What is claimed is:

1. A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer in the opening, the opening having an aspect ratio greater than about two, and wherein a portion of the opening not filled with said first dielectric layer has an aspect ratio of not greater than about two; and

forming a second dielectric layer over the first dielectric layer, the second layer having a top surface that is not within the opening.

2. The method of claim 1, further comprising providing a substrate before forming the opening.

3. The method of claim 2, wherein providing the substrate includes providing a substrate selected from the group consisting of a silicon substrate, an insulator substrate, and a sapphire substrate.

4. The method of claim 1, wherein forming a first dielectric layer includes forming the first dielectric layer having a top surface that is not within the opening.

5. The method of claim 1, wherein forming a first dielectric layer includes forming the first dielectric layer having a top surface that is within the opening.

6. The method of claim 1, wherein:

forming a first dielectric layer includes forming the first dielectric layer through an ozone-TEOS deposition; and

forming a second dielectric layer includes forming the second dielectric layer through an ozone-TEOS deposition.

7. The method of claim 1, wherein:

forming a first dielectric layer includes forming the first dielectric layer at a first process setting; and

forming a second dielectric layer includes forming the second dielectric layer at a second process setting at a predetermined relationship with the first process setting.

8. The method of claim 7, wherein the first process setting and the second process setting are selected from the group consisting of temperature, reactor chamber pressure, dopant concentration, flow rate, and shower head spacing.

9. The method of claim 1, wherein:

forming a first dielectric layer includes forming the first dielectric layer at a first temperature; and

forming a second dielectric layer includes forming the second layer at a second temperature, the second temperature being less than the first temperature.

10. The method of claim 1, wherein:

forming a first dielectric layer includes forming the first dielectric layer at a first pressure; and

forming a second dielectric layer includes forming the second dielectric layer at a second pressure, the second pressure being greater than the first pressure.

11. The method of claim 1, wherein:

forming a first dielectric layer includes forming the first dielectric layer at a first dopant concentration; and

forming a second dielectric layer includes forming the second layer at a second dopant concentration, the first dopant concentration being less than the second dopant concentration.

12. The method of claim 1, wherein:

forming a first dielectric layer includes forming the first dielectric layer at a first total TEOS and dopant flow rate; and

forming a second dielectric layer includes forming the second layer at a second total TEOS and dopant flow rate, the first total TEOS and dopant flow rate being less than the second total TEOS and dopant flow rate.

13. The method of claim 1, wherein:

forming a first dielectric layer includes:

providing a shower head at a first distance from the substrate, and

providing through the shower head constituents forming the first layer;

and

forming the second dielectric layer includes:

providing the shower head at a second distance from the substrate, the second distance lower than the first distance, and

providing through the shower head constituents forming the second layer.

14. A method of forming a dielectric layer during the manufacture of a semiconductor device, comprising:

providing a substrate;

forming an opening relative to the substrate, the opening having an aspect ratio greater than about two;

forming a first dielectric layer in the opening wherein a portion of the opening not filled with said first dielectric layer has an aspect ratio of not greater than about two; and

forming a second dielectric layer over the first dielectric layer, the second layer having a top surface that is not within the opening.

15. The method of claim 14, wherein forming an opening includes forming an opening in the substrate.

16. The method of claim 14, wherein forming an opening includes forming an opening on the substrate.

17. The method of claim 14, wherein forming an opening includes forming a plurality of structures on the substrate so that said plurality of structures forms an opening.

18. The method of claim 17, wherein forming a plurality the structures includes forming a plurality of conductors.

19. A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer in the opening, the first layer having a first process setting; and

forming a second dielectric layer over the first dielectric layer, the second layer having a top surface that is not within the opening and having a second process setting at a predetermined relationship with the first process setting.

20. The method of claim 19, wherein the first process setting and the second process setting are selected from the group consisting of temperature, reactor chamber pressure, dopant concentration, flow rate, and shower head spacing.

21. The method of claim 19, wherein the first process setting includes a first temperature, and the second process setting includes a second temperature, the first temperature being greater than the second temperature.

22. The method of claim 19, wherein the first process setting includes a first pressure, and the second process setting includes a second pressure, the first pressure being greater than the second pressure.

23. The method of claim 19, wherein the first process setting includes a first dopant concentration, and the second process setting includes a second dopant concentration, the first dopant concentration being less than the second dopant concentration.

24. The method of claim 19, wherein the first process setting includes a first flow rate, and the second process setting includes a second flow rate, the first flow rate being less than the second flow rate.

25. The method of claim 19, wherein the first process setting includes:

providing a shower head at a first distance from the substrate, and

providing through the shower head constituents forming the first layer; and

said second process setting includes:

providing the shower head at a second distance from the substrate, the second distance lower than the first distance, and

providing through the shower head constituents forming the second layer.

26. A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer completely filling the opening, the opening having an aspect ratio greater than about two; and

forming a second dielectric layer over the first dielectric layer.

27. A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer in the opening, the first layer being formed at a first temperature; and

forming a second dielectric layer over the first dielectric layer, the second layer having a top surface that is not within the opening and being formed at a second temperature, the first temperature being greater than the second temperature.

28. A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer in the opening, the first layer being formed at a first pressure; and

forming a second dielectric layer over the first dielectric layer, the second layer having a top surface that is not within the opening and being formed at a second pressure, the first pressure being greater than the second pressure.

29. A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer in the opening, the first layer having a first dopant concentration; and

forming a second dielectric layer over the first dielectric layer, the second layer having a top surface that is not within the opening and having a second dopant concentration, the first dopant concentration being less than the second dopant concentration.

30. A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer in the opening, the first layer being formed at a first flow rate; and

forming a second dielectric layer over the first dielectric layer, the second layer having a top surface that is not within the opening and being formed at a second flow rate, the first flow rate being less than the second rate.

31. A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer in the opening, said forming the first layer including:

providing a shower head at a first distance from the substrate, and

providing through the shower head constituents forming the first layer; and

forming a second dielectric layer over the first dielectric layer, the second layer having a top surface that is not within the opening, said forming the second layer including:

providing the shower head at a second distance from the substrate, the second distance lower than the first distance, and

providing through the shower head constituents forming the second layer.

32. An assembly, comprising:

a substrate;

an opening relative to said substrate, said opening having an aspect ratio greater than about two;

a first dielectric layer in said opening wherein a portion of said opening not filled with said first dielectric layer has an aspect ratio of not greater than about two; and

a second dielectric layer over said first dielectric layer, said second layer having a top surface that is not within said opening.

33. The assembly of claim 32, wherein said opening is formed from a plurality of structures on said substrate.

34. The assembly of claim 32, wherein said first dielectric layer is selected from a group consisting of silicon oxide, TEOS oxide, silicon nitride and oxynitride.

35. The assembly of claim 32, wherein said second dielectric layer is selected from a group consisting of silicon oxide, TEOS oxide, silicon nitride and oxynitride.

36. The assembly of claim 32, wherein said first layer includes a top surface that is within said opening.

37. The assembly of claim 32, wherein said first layer includes a top surface that is not within said opening.

38. The assembly of claim 32, wherein said assembly forms a portion of a device selected from a group consisting of a transistor, a capacitor, a logic circuit, a memory array, a memory device, and a processor.

39. An assembly, comprising:

a plurality of structures forming an opening, said opening having an aspect ratio greater than about two;

a first dielectric layer in said opening wherein a portion of said opening not filled with said first dielectric layer has an aspect ratio of not greater than about two; and

a second dielectric layer over said first dielectric layer, said second layer having a top surface that is not within said opening.

40. The assembly of claim 39, wherein said plurality of structures are conductors.

41. The assembly of claim 40, wherein said plurality of structures are selected from a group consisting of aluminum and polysilicon.

42. The assembly of claim 39, wherein said plurality of structures are parallel conductors.

43. The assembly of claim 39, wherein said plurality of structures are stepped structures.

44. The assembly of claim 39, wherein said plurality of structures include sidewalls defining said opening.

45. The assembly of claim 39, wherein said assembly forms a portion of a device selected from a group consisting of a transistor, a capacitor, a logic circuit, a memory array, a memory device, and a processor.

46. The assembly of claim 39, wherein said plurality of conductors are formed on a substrate.

47. An assembly, comprising:

a plurality of conductors forming an opening, said opening having an aspect ratio greater than about two;

a first dielectric layer in said opening wherein a portion of said opening not filled with said first dielectric layer has an aspect ratio of not greater than about two ; and

a second dielectric layer over said first dielectric layer, said second layer having a top surface that is not within said opening.

48. The assembly of claim 47, wherein said conductors are parallel conductors.

49. An assembly, comprising:

a substrate;

an opening relative to said substrate, said opening having an aspect ratio greater than about two;

a first ozone-TEOS layer in said opening wherein a portion of said opening not filled with said first dielectric layer has an aspect ratio of not greater than about two; and

a second ozone-TEOS layer over said first layer, said second layer having a top surface that is not within said opening.

50. An assembly, comprising:

a plurality of structures forming an opening, said opening having an aspect ratio greater than about two;

a first ozone-TEOS layer in said opening wherein a portion of said opening not filled with said first dielectric layer has an aspect ratio of not greater than about two; and

a second ozone-TEOS layer over said first layer, said second layer having a top surface that is not within said opening.

51. A system, comprising:

a first device including a substrate, an opening relative to said substrate, said opening having an aspect ratio greater than about two, a first dielectric layer in said opening wherein a portion of said opening not filled with said first dielectric layer has an aspect ratio of not greater than about two, a second dielectric layer over said first dielectric layer, said second layer having a top surface that is not within said opening;

a second device; and

a bus connected to both said first device and said second device.

52. The system of claim 51, wherein said first device is selected from a group consisting of a transistor, a capacitor, a logic circuit, a memory array, a memory device, and a processor.

53. The system of claim 51, wherein said first device is a memory device and said second device is a memory device.

54. A system, comprising:

a first device including a plurality of structures forming an opening, said opening having an aspect ratio greater than about two, a first dielectric layer in said opening wherein a portion of said opening not filled with said first dielectric layer has an aspect ratio of not greater than about two, and a second dielectric layer over said first dielectric layer, said second layer having a top surface that is not within said opening;

a second device; and

a bus connected to both said first device and said second device.

55. The system of claim 54, wherein said first device is selected from a group consisting of a transistor, a capacitor, a logic circuit, a memory array, a memory device, and a processor.

56. The system of claim 54, wherein said first device is a memory device and said second device is a memory device.

57. The system of claim 54, wherein said plurality of structures in said first device are formed on a substrate.